



Preliminary Program Overview, rev2.5 *(Subject to updates and changes)*

	DAY 1: December 2, 2025
8:00am - 9:00am	Registration & Refreshment
Venue	Resort World West Ballroom at Basement 2
9:00am - 9:10am	Welcome Speech: Dr Eric Phua, EPTC 2025 General Chair
9:10am - 9:20am	Opening Speech: Prof Jeffery Suhling (EPS President-Elect)
9:20am - 10:05am	Keynote 1: Dr Radha Nagaranjan, SVP/CTO, Marvell
10:05am - 10:25am	20min Coffee Break @ West Ballroom Foyer
10:25am - 11:10am	Keynote 2: Audrey Charles, SVP, Lam Research
11:10am - 12:10pm	Panel Session: Advances and Challenges in Metrology and Test for Heterogeneous Integration Moderator: Sia Choon Beng (FormFactor)
12:10pm - 12:30pm	Technology Solution Presentation: by Lam Research (Diamond Sponsor)
Venue	West Ballroom Foyer
12:30pm - 1:30pm	Lunch @ West Ballroom Foyer
	Exhibition Hall Opens (LEO 1-4 Function Room at Level 1)
Venue	Resort Worlds West Ballroom at Basement 2
1:30pm - 2:15pm	Keynote 3: Pax Wang, TD Director, UMC
2:15pm - 2:30pm	Technology Solution Presentation: by Applied Materials (Platinum Sponsor)
2:30pm - 3:15pm	Keynote 4: Prof. Harald Kuhn, Director, Fraunhofer Institute of Electronic Nano Systems ENAS
3:15pm - 3:40pm	20min Coffee Break @ West Ballroom Foyer
3:40pm - 3:55pm	Technology Solution Presentation: by KLA-Tencor (Platinum Sponsor)
3:55pm - 4:55pm	Panel Session: Co-Packaged Optics: The Next Inflection Point for Advanced Packaging Moderator: Surya Bhattacharya (IME)
4:55pm - 5:45pm	Day 1 Wrap-Up and Networking Reception @ Outside West Ballroom
6:30pm - 8:00pm	VIP Dinner @ Tangerine, Equarius Hotel (by invitation only)

	DAY 2: December 3, 2025					
Venue	Aquarius 2 & 3	Aquarius 4	Gemini 1	GEMINI 2	Pisces 1	Pisces 2
08:30am - 10:00am	PDC1	PDC2	PDC3	PDC4	PDC5	PDC6
	Advanced Packaging for Chiplets, Heterogenous Integration and CPO Dr John Lau (Unimicron)	Photonic Components and Packaging Technologies for Data Center, Communications, Sensing and Displays Dr Torsten Wipiejewski (Huawei)	Advanced Packaging for MEMS and Sensors Dr Horst Theuss (Infineon)	Current and Future Challenges and Solutions in AI & HPC System and Thermal Management Dr Gamal Refai-Ahmed (AMD)	Overview of Characterization Techniques for 3D HI Circuit Packaging Prof Ali Shakouri (Purdue University)	Design-on Simulation Technology for Reliability Prediction of AP Prof K.N. Chiang (National Tsing Hua University)
10:00am - 10:30am	30min Coffee Break outside Exhibition Hall (LEO 1-4)					
10:30am - 12:00pm	PDC1 (con't)	PDC2 (con't)	PDC3 (con't)	PDC4 (con't)	PDC5 (con't)	PDC6 (con't)
12:00pm - 1:15pm	EPS Luncheon @ PISCES 2 to Virgo 3					
1:15pm - 2:25pm	Technology Innovation Showcase - Session 1 (70 min) Quiz & Prizes Included					
Venue	Aquarius 3	Aquarius 4	Gemini 1	Gemini 2	Pisces 1	Pisces 2
2:25pm - 3:10pm	Materials and Processing 1	TSV/Wafer Level Packaging 1	Mechanical Simulation & Characterization 1	Interconnection Technologies 1	Advanced Packaging 1	Emerging Technologies
2:25pm - 2:40pm	P372 (111)-Oriented Nanotwinned/ Nanograined Bilayer Cu for Post-Q-time Low Temperature Cu-Cu Bonding	P168 Thermally Reliable Through Glass Via Filling with Ni-Fe Alloy for Advanced 3D Packaging (MAT)	P317 Toward lifetime prediction under variable load conditions in power electronics	P266 Surface Treatment for Wafer Bonding using Atmospheric Vapor Plasma Technology	P170 Development of Embedded Bridge Die interposer Using FO Packaging for HI of NPUs and HBMs	P326 3D Surface Ion Trap Process Development for Quantum Applications
	Peng, Gangqiang City University of Hong Kong, Hong Kong	Yang, Fan Hanyang University, Korea	Horn, Tobias Daniel Micro Materials Center, Fraunhofer ENAS, Chemnitz, Germany	Choi, Won Young Samsung Electronics, Korea	Kim, Jay nepes, Korea	Li, Hongyu Institute of Microelectronics, A*STAR, Singapore
2:40pm – 2:55pm	P167 Enhancing Wafer Bonding Strength via Surface and Dielectric Modification Using Plasma Activation Process	P319 RDL-first FOWLP Development for III-V Semiconductor Chips in RF Applications	P255 Board level solder reliability and package stress for TSICV UBM/bump IC package design	P185 Study of Extremely Low Temperature Organic Hybrid Bonding with Grain Engineered Cu	P287 HI of High-Performance Compute, Memory and Photonic Engine Chiplets on Large Molded Interposer package	P161 2.5D Cryogenic Packaging for Advanced Quantum Processors
	Park, Jaehyung Samsung Electronics, Korea	Ho, Soon Wee David Institute of Microelectronics, A*STAR, Singapore	Mandal, Rathin Institute of Microelectronics, A*STAR, Singapore	Maruyama, Yoshiki Resonac Corporation	Chai, Tai Chong Institute of Microelectronics, A*STAR, Singapore	Jaafar, Horhanani Institute of Microelectronics, A*STAR, Singapore
2:55pm – 3:10pm	P356 Analysis of SiO ₂ surface chemistry by quasi-in situ XPS during N ₂ plasma activation for SiO ₂ /SiO ₂ bonding	P302 Mitigating Connected PAD Corrosion in Hybrid Bonding	P138 Design of Wire Bonding Schemes for Reliability of CQFP Packages under Vibration Test	P355 Bond line thickness stability of Cu sintering for automotive power module packaging	P199 Ultra-low-TTV Glass Carrier and Temporary Bonding Method to Enable Wafer Ultra-thinning	P208 Wafer-level Processes for the Manufacturing of Encapsulated Flexible Polymer-Based Implants
	Yang, Haibo Institute of Microelectronics of the Chinese Academy of Sciences, China	Chew, Soon Aik IMEC, Belgium	Ma, Yiyi STMicroelectronics, Singapore	Kim, Byeongchan Korea Institute of Industrial Technology, Korea	Chang, Ya Huei Corning incorporated	Gao, Jiaying Huawei Device, China

	DAY 2: December 3, 2025 (con't)					
3:10pm - 4:40pm	Interactive Presentation 1 (Poster), Exhibition and Coffee Break outside Exhibition Hall (LEO 1-4)					
Venue	Aquarius 3	Aquarius 4	Gemini 1	Gemini 2	Pisces 1	Pisces 2
4:40pm -5:40pm	Materials and Processing 2	Thermal Management and Characterization 1	Mechanical Simulation & Characterization 2	Interconnection Technologies 2	Advanced Packaging 2	Assembly and Manufacturing Technology 1
4:40pm – 4:55pm	P343 Chip Stacking: Impact of Chip Spacing in C2W hybrid bonding on Temporary Bonding and Debonding Sharma, Jaibir Institute of Microelectronics, A*STAR, Singapore	P251 DIMM Thermal Performance Enhancement with Heat Spreader and Advanced Cooling Solutions Nallavelli, Ramesh Micron Technology Operations India LLP	P241 Electric-Thermal Coupled Transient Simulation for a Schottky Diode with Temperature Dependent Resistivity of Epitaxial Layer Yahaya, Khairul Ikhsan Nexperia Hong Kong	P188 A Novel Interface Characterization Technique for Hybrid Bonding Process Optimization Saito, Masahiro Toray Research Center, Inc., Japan	P354 Innovation and Efficiency in 3D Packaging Enabled by Optimized Integration Processes Varga, Ksenija EV Group, Austria	P201 High-Density Interconnect RDL-FPC Hybrid Substrate for Compact SiP Packaging Li, Jeng-Ting Unimicon Technology Corp., Taiwan
4:55pm – 5:10pm	P382 Water Vapor Permeation in Low-Temperature Processable Polyimide Materials for Reliable Polymer HB Nomura, Kota Toray Industries Inc., Japan	P223 CFD and Surrogate Model-Driven Optimization of Two-Phase Immersion Cooling Configurations Jalali, Ramin National Yang Ming Chiao Tung University	P332 Prediction of Void-induced Crack Propagation within Underfill using the Meshless Material Point Method de Jong, Sjoerd Douwe Medard Delft University of Technology	P174 Gas-Free & Nano TiO2-Coated Ag Bonding Wire for Replacing Au Wire Park, Soojae OxWires Co., Ltd., Korea	P275 Seamless Heterointegration of Components: Advancements in Fanout Technology and Thermal Solutions in SiP Gernhardt, Robert Fraunhofer IZM, Germany	P365 Novel UV-USP Laser Grooving and Plasma Dicing Separation Schemes for Next Generation Advanced Packaging Evertsen, Rogier ASMPT ALSI, The Netherlands
5:10pm – 5:25pm	P165 Novel TIM1 paste for Enhanced Thermal Management Liao, Yile Heraeus Materials Pte Ltd, Singapore	P153 Thermal Design and Power Dissipation of Advanced Package with Heterogenous Integration Han, Yong Institute of Microelectronics, A*STAR, Singapore	P271 Enhancing Predictive Accuracy of Warpage and Reliability for Advanced Packages by Modelling Accurate Poisson's Ratio in FEM Che, Faxing Micron Semiconductor Asia Operations Pte. Ltd	P280 High-AR, Fine-Pitch Through-Mold Interconnect Fabrication for Heterogeneous Integration of HPC Chia, Lai Yee Institute of Microelectronics, A*STAR, Singapore	P102 A Packaging Structure for an Antenna-in-Package Module Tain, Ra-Min Unimicon Technology Corporation, Taiwan	P173 Is Flash Lamp Annealing a Relevant Wafer Debonding Technique? Jedidi, Nader IMEC, Belgium
5:25pm – 5:40pm	P362 Applicability of Both-Sided Flash Lamp Annealing (FLA) Method on Heat Treatment Cu Plating Thin Film and Low Dielectric Resin Films Noh, Joo-Hyong Graduate School of Engineering, Kanto Gakuin University	P142 PIV-Based Study of Heat Dissipation and Clogging phenomenon of TiO₂ Nanofluid in Microchannels Li, Tieliang Xidian University, China	P294 Optimization of Warpage and Mechanical Properties for Stacked SiP Package Liu, Zhen Changsha AnMuQuan Intelligent Technology Co., Ltd, China	P144 Interfacial Reactions of BiIn and SnBi Solders React with Cu Substrate Wang, Yi-Wun Tamkang University, Taiwan	P303 Using WGAN-Based Data Augmentation Machine Learning Algorithm for Estimating the Equivalent Material Properties Su, Qinghua National Tsing Hua University, Taiwan	P301 Cost efficient Infrared Laser debonding technology enabled by Si carrier reuse Chancerel, Francois IMEC, Belgium
5:40pm - 6:45pm	Sponsors/Exhibitors Appreciation and Networking Cocktail Session @ Virgo 4					

	DAY 3: December 4, 2025					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
8:45am -9:45am	TSV/ Wafer Level Packaging 2	Smart Manufacturing and Equipment Technology 1	Mechanical Simulation & Characterization 3	Quality, Reliability & Failure Analysis 1	Advanced Packaging 3	Assembly and Manufacturing Technology 2
8:45am – 9:00am	P106 Adaptive Patterning®: Unlocking Scalable Density in Embedded Bridge Die Interposer	P242 Connectivity-Guided Feasibility Masking for Efficient Chiplet Placement in 2.5D Packaging via Reinforcement Learning	P177 Study on the Warpage Simulation and its Validation of Lidded FCBGA with Indium alloy TIM	P140 Studies and Elimination of F- induced Corrosion on AI Bondpads and Wafer Fabrication Process Improvement	P312 Characterization of PVD Seed Layer Contact Resistance in 2.0 to 20.0 µm Vias	P273 Selective Post-Soldering Volume Adjustment for Improved Co-Planarity of C4 Bump Interfaces
	Sandstrom, Clifford Paul Deca Technologies, United States of America	Kundu, Partha Pratim Institute for Infocomm Research (I2R), A*STAR, Singapore	Park, Yoonsoo Amkor technology, Inc., Korea	Hua, Younan WinTech Nano-Technology Services Pte. Ltd., Singapore	Carazzetti, Patrik Evatec AG, Switzerland	Fettke, Matthias PacTech GmbH, Germany
9:00am – 9:15am	P336 Novel Selective Copper Deposition Method for TGV Filling	P263 Real-Time 3D Reconstruction for Wire Bonding Using Multi-View Projection and EM Polynomial Modelling	P233 A Shock Vibration Calculation Method Considering Viscoplastic Behavior of Packaging Systems	P228 Annealing effect for Backside Metallization of SiC device	P150 112 Gbps SERDES Channel Design with 2.5D Sub-Micron BEOL Interconnect	P178 Aerosol Jet Printing of a Copper Nanoparticle Ink by Controlling the Wetness of Aerosols
	Seo, Jong Hyun Cuprum Materials Inc., Korea	Lin, Chih Hui ASMPT, Taiwan	Chen, Honghao Nanjing University of Posts and Telecommunications	Sameshima, Junichiro Toray Research Center, Inc., Japan	Gowda, Vinay Ramachandra Applied Materials, United States of America	Zheng, Cheng Nanyang Technological University, Singapore
9:15am – 9:30am	P172 Thin Fan-Out Package Characterization and Evaluation	P186 Defect Localization in Material Surfaces Using retinal CSRF kernel and Statistical Peak Profiling	P113 Delamination Effect Investigations Near RDL and UBM in WLCSP Packages	P306 Direct Bonding of Aluminum and Polypropylene in High- Reliability Structural Interfaces	P151 Advanced Bevel Deposition for Enhanced Yield and Cost Efficiency in Wafer-Level Bonding	P162 Heat Release Tape Characterization for Panel Level Packaging
	Lin, Vito Siliconware Precision Industries Co., Ltd., Taiwan	Hanmante, Udaykumar Applied Materials	Huang, Leo Renesas, Taiwan	Park, Jin Woong Hanbat National University, Korea	Xiao, Yun Lam Research, China	Shanmuga Sundaram, Shanthini ST Microelectronics, Singapore
9:30am – 9:45am	P111 Process-induced parasitic surface conduction (PSC) in SOI substrates for 3D-integrated RF front-end applications	P187 Enhancing Wire Bonding Quality Prediction with a Physics- Informed Ensemble Learning Framework	P368 Feasibility Study of Stacked Sub-THz Band AiP Modules Based on Warpage and Stress Analysis	P219 Nanoindentation tests and constitutive study of sintered nano- silver	P307 Physics-Informed Graph Convolutional Neural Network for Scalable, and Accurate Thermal Analysis of 2.5D Chiplet-based Systems	P175 Reliability Evaluations of Pb- free Solder Joint Formed Using Sn- Ag-Cu solder ball and Sn-Bi-Ag solder paste
	Rotaru, Mihai Dragos Institute of Microelectronics ASTAR, Singapore	Lu, Hsin-Fang ASMPT Limited, Taiwan	Tsukahara, Makoto SHINKO ELECTRIC INDUSTRIES CO., LTD., Japan	Yu, Huachen Nanjing University of Posts and Telecommunications, China	Sahay, Rahul Singapore University of Technology and Design, Singapore	Kim, Jahyeon Korea Institute of Industrial Technology (KITECH), Hanyang University, Korea
9:45am -10:15am	30min Coffee Break outside Exhibition Hall (LEO 1-4)					
10:15am -10:45am	Invited Talk 1: Dr Dielacher Bernd (EVG) The Critical Role of Wafer Bonding in Next-Generation Interconnect Scaling	Invited Talk 2: Dr Taku Hanna (ULVAC Inc) Polymer Fine Pattern Formation based upon Plasma Etching for High Density RDL Interposer	Invited Talk 3:	Invited Talk 4: Inohara Masahiro (KIOXIA) Accelerating the Evolution of NAND Flash Memory with Bonding Technologies	Invited Talk 5: Dr Mushuan Chan (SPIL) High Layer RDL Process Technology for Heterogenous Integration Package	Invited Talk 6: Dr Sajay BG (IME) Heterogeneously Integrated WL Processed CPO Engine for Next Gen AI/ML Data Centers
Venue	VIRGO 1-4					
10:45am - 11:55am	Technology Innovation Showcase Session 2 (70 min) Quiz & Prizes Included					
Venue	VIRGO 1-4					
11:55am -1:00pm	EPTC Luncheon @ PISCES 2 to VIRGO 3					

	DAY 3: December 4, 2025 (con't)					
11:55am -1:00pm	EPTC Luncheon					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
1:00pm -1:45pm	Materials and Processing 3	Thermal Management and Characterization 3	Mechanical Simulation & Characterization 4	Interconnection Technologies 3	Advanced Packaging 4	Quality, Reliability & Failure Analysis 3
1:00pm – 1:15pm	P164 Metallurgical properties of Sn-3.0Ag-0.5Cu solder joints with Alumina layer deposition	P191 Magnetohydrodynamic Liquid Cooling Embedded in PCBs for High-power Electronics	P252 Evaluating Dummy Die Sizes and Compound Adjustments to reduce Wafer Warpage in FOEB-T Packaging.	P202 Comparative wear-out study and characterization methods for Pure and Alloyed Copper wires	P320 Ka-Band Ultra-Short Die-to-Antenna Interconnect Enabled by Embedded Glass Fan-Out Packaging	P141 Short-Circuit Behavior and Failure Mechanism Analysis of Double-Trench SiC MOSFETs
	Noh, Eun-Chae Chungbuk National University, Korea	Feng, Huicheng A*STAR, Singapore	Zeng, TzuChi Siliconware Precision Industries Co., Ltd., Taiwan	Caputo, Onofrio Davide Università degli Studi di Milano-Bicocca, Italy	Jin, Shengxiang Peking University Shenzhen Graduate School, China	Zhang, Jiaju The Institute of Technological Sciences, Wuhan University, Wuhan, China
1:15pm – 1:30pm	P211 Wettability, Mechanical Properties and IMC of SiC nanoparticle-reinforced Sn-58Bi solders on Cu substrates under multiple reflow cycles	P247 Thermal Performance of MEMS Cross-flow Heat Exchangers Subjected to External Heat Transfer	P369 Characterization and Modelling of Inelastic Behavior of Epoxy Molding Compounds	P378 MDQFN™: Panel-Level QFN for Scalable, Cost-Effective Semiconductor Packaging	P227 Development of a Wideband Energy Harvesting Circuit Utilizing Terrestrial Digital Broadcast Signals	P276 A Modified Test Vehicle Incorporating DNP-Induced Strain Gradients for Single-Specimen Fatigue Life Assessment of Solder Joints
	Yao, Wang Harbin Institute of Technology	Alnaimat, Fadi United Arab Emirates University, United Arab Emirates	Tippabhotla, Sasi Kumar Institute of Microelectronics, A*STAR, Singapore	Davis, Robin Deca Technologies, Inc., United States of America	Tanaka, Hayato Kyushu University, Japan	Park, Hyeong-Bin Hanyang University, Korea
1:30pm – 1:45pm	P304 Impact of Solder Powder Size on Cleaning Efficiency in Chip Resistor Assemblies for Future Advanced Packaging	P270 Numerical Investigation of Embedded Micro-Pin Fin Two-Phase Liquid Cooling for Dual-Chip Stacks in HPC & AI Applications	P220 Nanoindentation Test and Crystal Plasticity Finite Element Model of SAC305 Solder Joint Considering Crystal Orientation	P157 Investigation of Cu bonding wire lifetime under accelerated temperature environments	P146 Optimization of Shielded Capacitive Power Transfer (S-CPT) Systems Using Slotted Electrodes	P147 Correlation Between Thermal Cycling Ramp Rates and its Respective Solder Joint Reliability
	Parthasarathy, Ravi ZESTRON Americas, United States of America	Patra, Chinmaya Kumar Indian Institute of Technology Kharagpur, India	Yu, Huachen Nanjing University of Posts and Telecommunications, Nanjing, China	Azuma, Shinya Nippon Micrometal Corporation, Japan	Chen, Hao Kyushu University, Japan	CHAN, Yong Tat STMicroelectronics Pte Ltd, Singapore
1:45pm - 3:15pm	Interactive Presentation 2 (Poster), Exhibition and Coffee Break outside Exhibition Hall (LEO 1-4)					

	DAY 3: December 4, 2025 (con't)					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
3:15pm -4:00pm	Materials and Processing 4	Thermal Management and Characterization 4	Mechanical Simulation & Characterization 5	Interconnection Technologies 4	Advanced Packaging 5	Assembly and Manufacturing Technology 3
3:15pm – 3:30pm	P379 Enhancing Yield Performance in Chip-to-Wafer Hybrid Bonding in Advanced Packaging	P371 Direct-Bonded Manifold-Jet-Impingement Cooling for High-Performance AI Chips	P352 Statistical Evaluation of Bond Strength Variation in Hybrid Bonding Interfaces	P299 Fluxless Die to Die Bonding of 10µm Ultra-fine Pitch Microbump	P367 Low Temperature Post Bond Anneal for Hybrid Bonding enabled by Interfacial (IF) Metal Capping – An Assessment of Reliability	P196 Growth Behaviour of Intermetallic Compounds in Cu-Sn3.5Ag Solder Joints with Different furnace cooling rate
	Xie, Ling Institute of Microelectronics, A*STAR, Singapore	Zhang, Yuantong Xi'an Jiaotong University, China	Kobayashi, Daiki YOKOHAMA National University, Japan	Xu, Zheqi Tsinghua University, China	Rath, Santosh Kumar Applied Materials Singapore, Singapore	Gan, Jingjian NXP Semiconductors, China
3:30pn – 3:45pm	P234 Study on Backside Metallization for the S-SWIFT(TM) Package	P334 High-Temperature Pressure Mapping of TIM Interfaces for Improved Thermal Simulation Accuracy	P349 Real-time Effective Mechanical Property Characterization of Redistribution Layer (RDL) for Chiplet Integration	P314 Novel Ultrasonic Flip Chip Bonding Approach utilizing electroplated Aluminium pillars for Advanced Packaging	P323 Backside Metal Interconnect for High Performance RF Interposer	P158 Hybrid Evaluation of Pure Argon Plasma Treatment for Enhanced Wire Bonding and Manufacturing Efficiency in Microelectronics
	Jo, Dambi Product Development Team, Amkor Technology, Korea	U, Srinath Cisco Systems (India) Private Limited, Bengaluru, India	Lu, Dingjie Institute of High-Performance Computing, A*STAR, Singapore	Cirulis, Imants Technical University Chemnitz, Fraunhofer ENAS, Germany	Lim, Teck Guan Institute of Microelectronics, A*STAR, Singapore	Pelingo, Jorell onsemi Carmona, Philippines
3:45pm – 4:00pm	P189 Study of Coverage Decay Mechanism of Liquid Metal Filler TIM for Advanced Package Application	P222 Operando Thermal Analysis of CPU and PCB using a Pixel-level Emissivity Correction Method	P274 Simulation and Validation of Warpage in Ultrathin Embedded-Die Substrates for Advanced Packaging	P353 Interfacial Electromigration Behavior and Reliability Evaluation in Cu/Ag Sintered Joints	P256 Surface Activation and Bonding Mechanisms of SiCN and TEOS Dielectrics for Low-Temperature Hybrid Bonding	P363 Comparative Evaluation of FCVA and High-Current Arc Deposited ta-C Films for Hermetic Encapsulation (Mat Paper)
	Jhan, Jyun-De Siliconware Precision Industries Co., Ltd., Taiwan	Kim, Seongjin Pohang University of Science and Technology (POSTECH), Korea	Ma, Rui Institute of Microelectronics of the Chinese Academy of Sciences, China	Kim, Yun-Chan Korea Institute of Industrial Technology, Korea University, Korea	Yang Haibo Institute of Microelectronics of the Chinese Academy of Sciences, China	Li, Ying Nanyang Technological University, Singapore

	DAY 3: December 4, 2025 (con't)					
Venue	VIRGO 1-4					
4:00pm - 5:10pm	Technology Innovation Showcase Session 3 (70 min) Quiz & Prizes Included					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
5:10pm - 5:55pm	Materials and Processing 5	Thermal Management and Characterization 5	Quality, Reliability & Failure Analysis 4	Interconnection Technologies 5	TSV/ Wafer Level Packaging 3	Assembly and Manufacturing Technology 4
5:10pm – 5:25pm	P116 Study on Microstructural Evolution Mechanisms of Amorphous SiO2 in Through Glass Via Wafer during Thinning Xu, Kezhong Huazhong University of Science and Technology, China	P163 Thermal Performance Enhancement of Stacked Packages using Silicon-Based Heat Spreading Die Lee, Seokjun Daniel Semiconductor R&D Center, Samsung Electronics, Korea	P115 Defect Z-depth Determination in 2.5D IC Using Magnetic Field Imaging Jayabalan, Jayasanker National University of Singapore, Singapore	P261 Microstructure Evaluation of Engineered Cu for Low-Temperature Cu-Cu Hybrid Bonding Tanaka, Fabiana Lie Yokohama National University, Japan	P105 Analysis of Cu and dielectric layer interfacial delamination in chip redistribution layer Yan, Yicheng Wuhan University, China	P315 Automated In-Line Metrology of Advanced Package Interconnections using a High-Speed 3D X-ray System Gregorich, Thomas Zeiss SMT, United States of America
5:25pm – 5:40pm	P272 Optimizing SSD Performance with One-Part Thermal Gap Fillers: A Sustainable Approach Kumaresan, Vigneshwarram SanDisk Storage Malaysia, Malaysia	P381 Solid-State On-Chip Thermal Management Using Micro-Thermoelectric Devices Kim, Jeong-Hwan Korea Advanced Institute of Science and Technology, Korea	P200 In-Situ Package Level Relative Humidity Measurement using Wet-Bulb and Dry-Bulb Temperatures Iyer, Vidya Subramanian Infineon Technologies Asia Pacific; Nanyang Technological University, Singapore	P179 A Molecular Dynamics Study of Grain Size Effects on Cu-Cu Interfacial Void Reduction in Direct Bonding Interconnect Park, Junhyeok Ulsan National Institute of Science and Technology, Korea	P126 Mitigation of Cu Nodule Formation in High Open Area Products for Electroplated Cu RDL Applications Lin, SW Lam Research Corporation, Taiwan	P224 Mass Transfer solution for Micro-LEDs based displays Wu, Jia Qi Institute of Microelectronics, A*STAR, Singapore
5:40pm 5:55pm	P316 Cost-Effective Wafer Level Micro Bumping Solution for Advanced Packaging P A, Mani Siva Heraeus Materials Singapore Pte Ltd, Singapore	P322 Thermal Sensitivity Analysis of SoIC Face-to-Back Stacking Using Foundation Models for Physics Kabaria, Hardik Vinci4D.ai Inc, USA	P358 AI-empowered 3D X-ray analysis of solder joint cracking after board level vibration testing Ghorbani, Amir Tu Delft, Netherlands	P243 In-situ AFM Analysis of Thermal Expansion of Cu Pads with Varied Grain Characteristics Yang, Gangli School of Integrated Circuits, Southeast University, China	P265 Characterization on Fan-Out Heterogeneous Integration Packaging for Premium Smartphone Chen, Cheng Chia Siliconware Precision Industries Co., Ltd., Taiwan	P118 Enhancing Electrochemical Migration Resistance of Sintered Silver by Ceria Additives for Die Attachment Applications Siow, Kim Shyong Universiti Kebangsaan Malaysia
06:15pm - 08:30pm	Party @ Ola Beach (ticketed event)					

	DAY 4: December 5, 2025					
Venue	VIRGO 1-4					GEMINI 2
8:45am – 10:00am	Technology Innovation Showcase Session 4 (75 min) Quiz & Prizes Included					R10 EPS Chapter Officers's Meeting
10:00am - 11:00am	60min Coffee Break outside Exhibition Hall (LEO 1-4)					
Venue	PISCES 1	PISCES 2	PISCES 3	PISCES 4	GEMINI 1	GEMINI 2
11:00am -11:30am	Invited Talk 7: Dr Kathy Yan (TSMC) From Cloud AI to Edge AI: Driving Innovation with Advanced Packaging	Invited Talk 8: Dr Takenori Fujiwara (Toray) Polymer Bonding Technology for Semiconductor Advanced Packaging	Invited Talk 9: Dr Tan Yik Yee (Yole Group) AI Is Accelerating the Shift to Advanced Packaging with FOPLP	Invited Talk 10: Jonathan Abdilla (BESI) Hybrid Bonding and Fluxless TCB: Defining the Sub 10um Interconnect Roadmap for 3D HI	Invited Talk 11: Dr Fu Chao (WinTechNano) Labless Enable Effective FA of Electronics Packages through Scientific Approach	Invited Talk 12: Dr Zhao Yi (ZSCT) Advanced Packaging EDA's New Paradigm: Collaborative Innovation Revolution for Design-Simulation- Verification in the 2.5D/3D Era
11:30am – 12:15pm	Advanced Packaging 6	Materials and Processing 6	Smart Manufacturing and Equipment Technology 2	Interconnection Technologies 6	Quality, Reliability & Failure Analysis 5	Mechanical Simulation & Characterization 6
11:30am -11::45pm	P350 n77/n79 Antenna-plexer with BAW and Glass-IPD Technology for 5G Applications Park, Minsoo Korea Electronics Technology Institute, Korea	P240 Copper Pillar Bump FCBGA Underfill Process Characterization for Automotive Application Koey Poh Meng, Dominic NXP Semiconductors, Malaysia	P193 AI-driven Pixel-Level Defect Localization using Magnetic Current Images Aung, Aye Phyu Phyu Institute for Infocomm Research (I2R), A*STAR, Singapore	P143 UV-Assisted Fluxless Thermal- Compression Bonding Under Ambient Conditions Kim, You-Gwon Hanyang University, Korea	P132 Anomalyspy: A Generative Defect Localization in Semiconductor Packages, with X-ray Microscopy I Made, Riko Institute of Materials Research and Engineering (IMRE), Singapore	P321 Degradation Mechanism of Frequency Stability in MEMS Resonant Accelerometers Bie, Xiaorui Institute of CAS, China
11:45am -12::00pm	P308 Power and Performance Comparison between FPGA- Optics Integrated 3D SiP and equivalent board level test hardware Bhandari, Jugal Kishore LightSpeed Photonics Private Limited, Singapore	P212 Enhanced Reliability of Large BGA Assemblies for AI Server and HPC Application Chen, Xianfeng Alibaba Cloud Intelligence Group, China	P236 Research on Intelligent Prediction of 3D-IC Packaging Injection Molding Based on Machine Learning Yu, Huachen Nanjing University of Posts and Telecommunications, China	P244 Characterization of Fine Line Width/Spacing RF Interconnects for Co-Packaged Optics with High I/O Density Wu, Jia Qi Institute of Microelectronics, A*STAR, Singapore	P180 Cu/SiCN wafer-to-wafer hybrid bonding interface reliability down to 400 nm pitch Chery, Emmanuel imec, Belgium	P370 Dev of a Reproducible, Stable, and Scalable Eval Routine for Lifetime Assessment of Power and Microelectronic Devices Albrecht, Jan Fraunhofer ENAS; Germany
12:00pm- 12:15pm	P361 Process Developments of Chip-to-Wafer assembly with HPC and Photonics Chiplets on large RDL-first interposer Lim, Sharon Pei Siang Institute of Microelectronics, A*STAR, Singapore	P384 Development and Monitoring of Gold Electroplating Process on 300mm Wafer Level Tran, Van Nhat Anh Institute of Microelectronics, A*STAR, Singapore	P359 Cross-Domain Adaptation of Automated 3D X-ray Defect Detection from HBM to Optical Transceivers Wang, Jie Institute for Infocomm Research (I2R), A*STAR, Singapore	P117 Study on Solder Core Ball Using Sn-Bi Plating for Low-Temperature Bonding Kim, Hui Joong MKE, Korea	P375 Investigations on the Mutual Effects of Electromigration and Thermal Fatigue failures of TSV Interconnects Cheng Tian Zhangjiang Lab, China	P329 Advancing Electronic Package Reliability Analysis by Predicting Solder Joint Strain Patterns Using Neural Networks Meier, Karsten Technische Universität Dresden, Germany
Venue	VIRGO 1-4					
12:15pm -1:30pm	Conference Lunch					

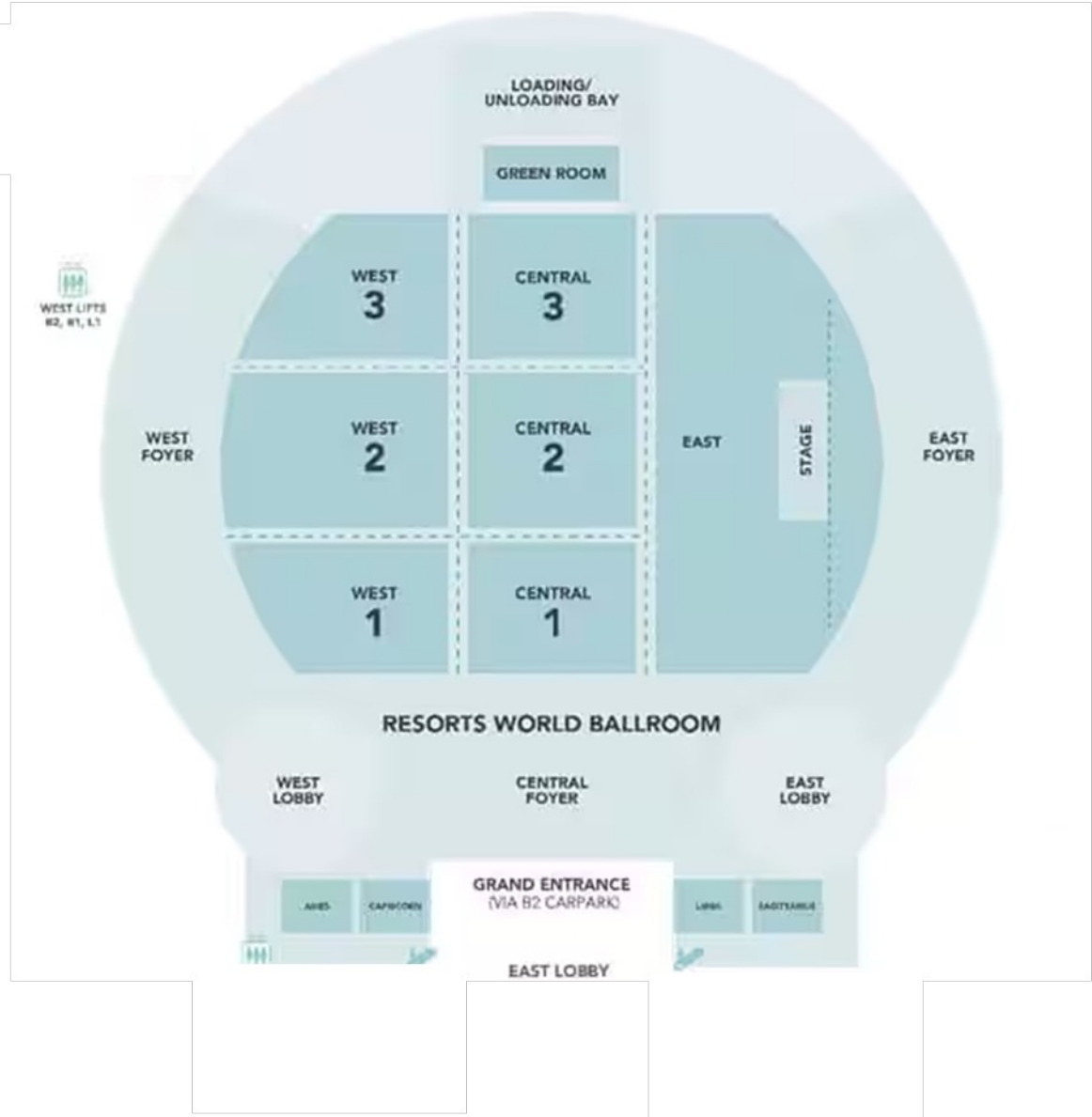
	DAY 4: December 5, 2025 (con't)					
12:15pm -1:30pm	Conference Lunch @ VIRGO 1 to 4					
Venue	PISCES 1	PISCES 2	PISCES 3	PISCES 4	GEMINI 1	GEMINI 2
	Advanced Packaging 7	Materials and Processing 7	Electrical Simulations & Characterization	Smart Manufacturing and Equipment Technology 3	Advanced Optoelectronics and Displays	Mechanical Simulation & Characterization 7
1:30pm - 1:45pm	P260 Demonstration of Integrated Passive Devices in Glass substrate using TGV process Yi, Sang-Ho Korea Electronics Technology Institute, Korea	P129 Pressure Sintering Mechanism of Ag Nanoparticles Based on The Master Sintering Curve and Visualization of Sinterability Hiratsuka, Daisuke TOSHIBA Corporation.	P169 Characteristics in the quasi-millimeter wave band of planar transmission lines formed on flexible substrates Kimigawa, Ryoma Kyushu University	P348 Inferring Wire Length and Depth from Magnetic Field Images via Deep-Spatial Physics Informed Model Jayavelu, Senthilnath Institute for Infocomm Research (I2R), A*STAR, Singapore	P267 Assembly of optical micro-ring resonator-based ultrasound sensor for photoacoustic imaging Lepukhov, Evgenii Tampere university, Finland	P139 Key Insights into Design for Reliability of 3D NAND Packages in Solid-State Drive Pan, Ling Micron Semiconductor Asia Pte Ltd, Singapore
	P154 Residue Free TaN Etch Method for MIM Capacitor in Advanced Packaging Zhou, Hexin Lam Research, China	P221 High-Performance Graphene Coatings for Superior Thermal and Mechanical Properties in Electronic Packaging Enclosures Sundararajan, Muralidharan SanDisk Storage Sdh Bhd, Malaysia	P289 Development of PDK Library for Accurate Modelling of 2.5D Interconnect Structures in Heterogeneous Integration Mani, Raju Institute of Microelectronics, A*STAR, Singapore	P213 Device-to-Package Electrothermal Performance Prediction of Power MOSFETs via Coupled Iterative Dual-Artificial Neural Networks Dai, Yuxuan Nanjing University of Posts and Telecommunications, China	P104 High Coupling Efficiency Adhesive for Photonic Packaging Lim, See Chian Garian DELO Industrial Adhesives	P373 A novel wafer warpage numerical model considering further shrinkage of epoxy molding compound Ji, Lin Institute of Microelectronics, A*STAR, Singapore
2:00pm - 2:15pm	Invited Talk 13 David Gani (STMicro) Challenges and Advantages in Panel Level Packaging	Invited Talk 14 Hidenori Abe (Resonac) Advanced Packaging Materials Innovation through Co-Creative Activities and Trends in Advanced Packaging Processes	Invited Talk 15: Dr Min Woo Rhee (Samsung) Understanding of Hybrid Bonding Mechanism by Utilizing Molecular Dynamics Approach	P209 Thermal- and Wirelength-Aware Chiplet Placement in 2.5D Systems Through Multi-Agent Reinforcement Learning Hou, Yubo Institute for Infocomm Research (I²R), A*STAR, Singapore	P253 2.5D PIC Photonic Interposer Engine for Next Generation Photonic Link CPO of High-Performance Computing and Data Communications Lee, Wen Institute of Microelectronics, A*STAR, Singapore	P127 Development of Warpage Predictive Models using Physics-Driven Simulation Yu, Wei Micron Semiconductor Asia Operations, Singapore
2:15pm - 2:30pm				P264 Generative AI-Powered Defect Detection for 3D X-ray Microscopy Scans of High Bandwith Memory Bumps Chang, Richard Institute for Infocomm Research (I2R), A*STAR, Singapore	P206 An Integrated Computational Materials Engineering approach for Anisotropic Conductive Films Gao, Jiaying Huawei Device, China	P239 Thermal and mechanical properties optimization of TGV interposer for 2.5D integrated transceiver Li, Chunlei Xiamen University; Sanming University, China
2:30pm – 3:00pm				30min Coffee Break outside Exhibition Hall (LEO 1-4)		

	DAY 4: December 5, 2025 (con't)
2:30pm – 3:00pm	30min Coffee Break outside Exhibition Hall (LEO 1-4)
Venue	VIRGO 1 to 3 (combined rooms)
3:00pm - 3:30pm	Heterogeneous Integration Roadmap (HIR) Workshop Theme: Interconnects - Design and Manufacturing of Complex HI Structures Opening: Kitty Pearsall Design for Manufacturability of > 1 kW: Gamal Refai Ahmed (AMD) Design – Photonics: Amr S Helmy (University of Toronto) Manufacturability – HBI: Loke Yuan Wong (Applied Materials) Manufacturability – Nelson Fan (ASMPT) Manufacturability – CPO (IME, A*STAR) Panel Discussion “Why HBI/CPO HVM Adaption is in Slower Pace Despite all the Buzz?” Moderator: Wong Shaw Fong (Intel)
3:30pm - 3:45pm	
3:45pm - 4:00pm	
4:00pm - 4:15pm	
4:15pm - 4:30pm	
4:30pm – 5:00pm	
5:10pm - 5:30pm	Closing Ceremony and Lucky Draw @ VIRGO 1, 2 and 3 (combined rooms)

Paper ID	Technical Committee	Authors	Affiliation
100	Advanced Packaging	Seyedmohammadi, Shahram	Henkel, United States of America
112	Advanced Packaging	Tateishi, Eiichi	Kyushu University Graduate School of Information Science and Electrical Engineering, Japan
114	Advanced Packaging	Wan Ahmad, Wan Mohd Alimie	NXP Semiconductors, Malaysia
128	Advanced Packaging	Volkovich, Roie	KLA, Israel
148	Advanced Packaging	Cheng, Ray	Lam Research, Taiwan
194	Advanced Packaging	Mohd Zali, Mohd Rozaini	Nexperia Malaysia Sdn Bhd, Malaysia
204	Advanced Packaging	Mühlstätter, Christian	EV Group, Austria
226	Advanced Packaging	Tseng, Chia-Wei	Graduate School of Advanced Technology, National Taiwan University, Taiwan
231	Advanced Packaging	Tschoban, Christian	Fraunhofer IZM, Germany
324	Advanced Packaging	Monroe, Matthew	Micron technology Inc., United States of America
333	Advanced Packaging	Zheng, Yuxiang	Institute of Microelectronics, Chinese Academy of Sciences
335	Advanced Packaging	Lian, Ziqi	Institute of Microelectronics of Chinese Academy of Sciences, Beijing
337	Advanced Packaging	Heinig, Andy	Fraunhofer IIS/EAS, Germany
257	Assembly and Manufacturing Technology	Zainal, Mohd Khairul	Nexperia Malaysia Sdn Bhd, Malaysia
295	Assembly and Manufacturing Technology	Rodriguez, Jenelyn	Infineon Technologies Asia Pacific Pte Ltd, Singapore
296	Assembly and Manufacturing Technology	Bartolo, Marlon	Infineon Technologies Asia Pacific Pte Ltd, Singapore
318	Assembly and Manufacturing Technology	Narayanasamy, Jayaganasan	PT. Infineon Technologies, Batam, Indonesia
338	Assembly and Manufacturing Technology	Soh, Serine	Institute of Microelectronics, Singapore
383	Assembly and Manufacturing Technology	Hu, Chao	Huazhong University of Science and Technology
107	Electrical Simulations & Characterization	Foo, Loke Yip	Altera, Malaysia
377	Electrical Simulations & Characterization	You, Wenchao	Beihang University, China
120	Emerging Technologies	Nakashima, Kenta	Kyushu University, Japan
262	Emerging Technologies	Otake, Yugi	Yokohama National University, Japan
130	Materials and Processing	Andriani, Yosephine	Infineon Technologies Asia Pacific Pte Ltd, Singapore
133	Materials and Processing	Buret, Mathilde	Inventec Performance Chemicals, France
134	Materials and Processing	Shrivastava, Saurabh	Macdermid Alpha Electronics Solutions India Private Limited, India
152	Materials and Processing	Cao, Danni	Central South University, Changsha, China
207	Materials and Processing	Zheng, Jiarui	Harbin Institute of Technology, China
216	Materials and Processing	LIU, YU	Heraeus Materials Singapore Pte. Ltd., Singapore
366	Materials and Processing	Pan, Manyi	Institute of Microelectronics, Singapore

Paper ID	Technical Committee	Authors	Affiliation
145	Quality, Reliability & Failure Analysis	Chen, Yong	STMicroelectronics, Singapore
171	Quality, Reliability & Failure Analysis	Ichikawa, Norimitsu	Kogakuin University, Japan
198	Quality, Reliability & Failure Analysis	Mori, Tomoki	YOKOHAMA National University, Japan
203	Quality, Reliability & Failure Analysis	NAMBA, Haruhito	Yokohama National University, Japan
205	Quality, Reliability & Failure Analysis	Shinomiya, Keisuke	Lintec corporation, Japan
214	Quality, Reliability & Failure Analysis	Tan, Tze Qing	Innovation, Heraeus Materials Singapore Pte. Ltd.
184	Smart Manufacturing Equipment Tech	Yu, Yang	Institute for Infocomm Research (I2R), Singapore
290	Smart Manufacturing Equipment Tech	Li, Mengyang	Institute of Microelectronics, Singapore
292	Smart Manufacturing Equipment Tech	Lestari, Yuli	INFINEON, Indonesia
124	Thermal Management & Characterization	RAVI, KAVITHA	Rajalakshmi Engineering College, India
225	Thermal Management & Characterization	Tseng, Chia-Wei	Graduate School of Advanced Technology, National Taiwan University, Taiwan
248	Thermal Management & Characterization	Huang, Jiapeng	Xiamen University, Xiamen, China
342	Thermal Management & Characterization	Liu, Cong	University of Electronic Science and Technology of China
357	Thermal Management & Characterization	Heinig, Andy	Fraunhofer IIS/EAS, Germany
121	TSV/Wafer Level Packaging	Chen, Zack	Lam Research, Taiwan
181	TSV/Wafer Level Packaging	Wang, Zhishen	Wuhan University, China
183	TSV/Wafer Level Packaging	Yang, Huihui	Lam Research, China
230	TSV/Wafer Level Packaging	Rathore, Shubham	Indian Institute of Technology Hyderabad, India
341	TSV/Wafer Level Packaging	Jl, Hongmiao	Institute of Microelectronics (IME), A*STAR, Singapore
123	Interconnection Technologies	PELINGO, JORELL	onsemi Carmona, Philippines
160	Interconnection Technologies	Manalo, Ginbert	onsemi Philippines, Philippines
245	Interconnection Technologies	Lin, Xiaoting	Shenzhen Advanced Joining Technology Co., LTD., China
278	Interconnection Technologies	Ong, Edward Yong Xi	Institute of Microelectronics, Singapore
288	Interconnection Technologies	DE JESUS, EDSEL	STMICROELECTRONICS, Singapore
330	Interconnection Technologies	Liu, Sichen	Beijing Institute of Technology, Beijing, China
331	Interconnection Technologies	Jedidi, Nader	imec, Belgium;
339	Interconnection Technologies	Sharma, Nishant	Indian Institute of Science, Bangalore, India
346	Interconnection Technologies	Dao, Thi Minh Anh	National Yang Ming Chiao Tung University, Taiwan
360	Interconnection Technologies	Xie, Yihan	Xiamen University, China
364	Interconnection Technologies	Singh, Avneesh	Indian Institute of Information Technology & Management Gwalior, India, India

Basement 2 Resort World Ballroom Floor Plan



Level 1 Exhibition and Breakout Room Floor Plan

